Application Note AN091

AS14x4 Design and Layout Guide

Rev 2.1
January 2018

TABLE OF CONTENTS

FIGURES

TABLES

ABOUT APPLICATION NOTE AN091

Application Note AN091 describes design and layout best-practices for implementing full system solutions on printed-circuit boards based around the Kinetic AS14x4 family of devices. Included are detailed recommendations for realizing a highly-integrated, low-noise, high-efficiency power system design in a compact form factor.

This design guide provides general guidelines for platform solutions utilizing the AS14x4 family of digital power controllers with integrated HV isolation and quad DC-DC outputs. These guidelines should be used in conjunction with the datasheet and reference design. The design guide provides information for adapting the reference design to a customer's system. If there are any questions of concerns, please contact the Kinetic applications team through your sales contact or sales@kinet-ic.com.

Refer to www.kinet-ic.com for further details on these and other Kinetic Technologies components.

INTRODUCTION TO SYSTEM DESIGN CONSIDERATIONS

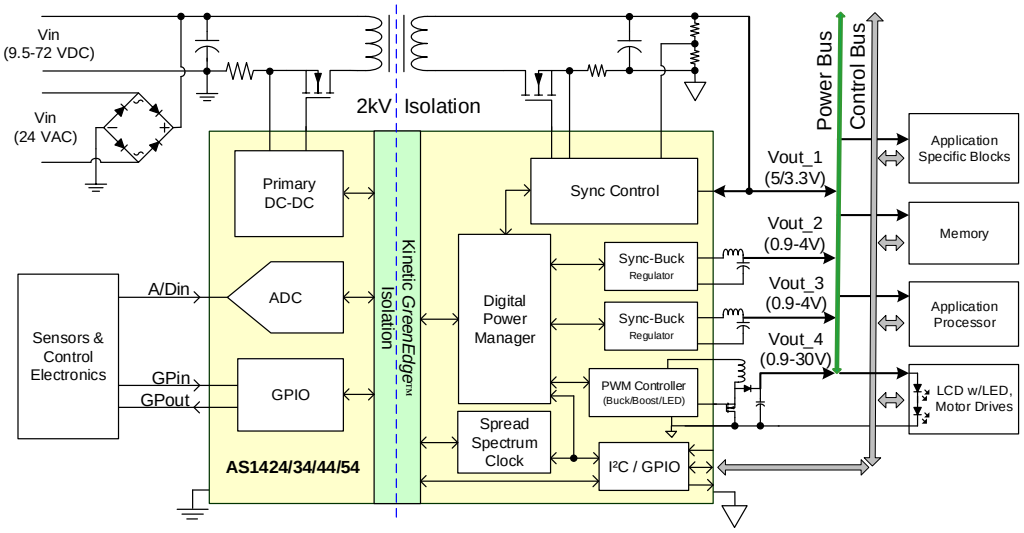
The AS1454/44/34/24 are Quad-Output Digital Power SoCs for 9.5-72VDC & 24VAC isolated power applications. All are built on Kinetic' integrated *GreenEdge*™ 2kV digital isolation technology creating a flexible power platform that eliminates all opto-couplers and minimizes component count and design footprint.

Synchronous converters with digital loop and timing control are integrated with digital isolation as part of an advance power system architecture for high-efficiency and cost-effective designs. Selectable spread-spectrum clocking on all PWMs reduces the power supply spectral noise for superior EMC performance. Bi-directional Isolated GPIO and isolated ADC ease system level design in many industrial and medical applications.

A Software compatible I²C management interface (AS1434 & AS1454 only) provides advanced power control and diagnostics capability. Hardware (pin) programmable device operation is available on all four devices.

As a result of the high level of integration, eliminating, for example, the need for opto-couplers, the AS14x4 provides fast dynamic response and enables robust protection from surge events through internal low-impedance discharge paths. The AS14x4 also limits stray surge currents from passing through sensitive circuits. Integrated isolation, moreover, enables the AS14x4 family to have superior efficiency performance across a wide load range.

Finally, the AS14x4 family implements many design features that minimize transmission of system common-mode noise onto the input power line.



Key features of the AS14x4 family are the following:

Four integrated high-efficiency, low-noise managed outputs.

- Fully-isolated, wide-input, 15W or 50W synchronous-flyback converter with integrated *Digital Edge*™ isolation technology, enhancing efficiency from low loading to high loading with precise primary-side and secondary-side FET timing control and improving bandwidth and system reliability by eliminating opto-couplers.
- Two synchronous DC-DC regulators with integrated MOSFETs (2A outputs).
- One PWM controller to drive external MOSFETs to generate a high-current buck or boost converter.

- I²C Interface uses *Digital Edge*™ isolation technology to monitor, control and manage primary-side and secondary-side signals.

GROUNDING

Because the AS14x4 IC has integrated isolation, proper grounding is paramount as with any isolated system. Figure 1 shows the pin diagram for the AS14x4. On the underside of the QFN package are three ground pads: PGND (Paddle#1), PGND (Paddle#2), and SGND (Paddle#3). Both the PGND (Paddle#1, 2) serves as the input power return. Please make sure to short both the PGNDs on PWB. Finally, SGND (Paddle#3) serves as the secondary-side ground connection.

In order to mitigate EMI, two 4.7nF/2kV capacitors should be connected between 48N and SGND. In terms of capacitor placement, it is recommended that one capacitor be placed underneath the IC on the back side directly across the paddles and that the other capacitor be placed next to the transformer. Additional capacitance may be required for applications which expose the IC to high RF fields.

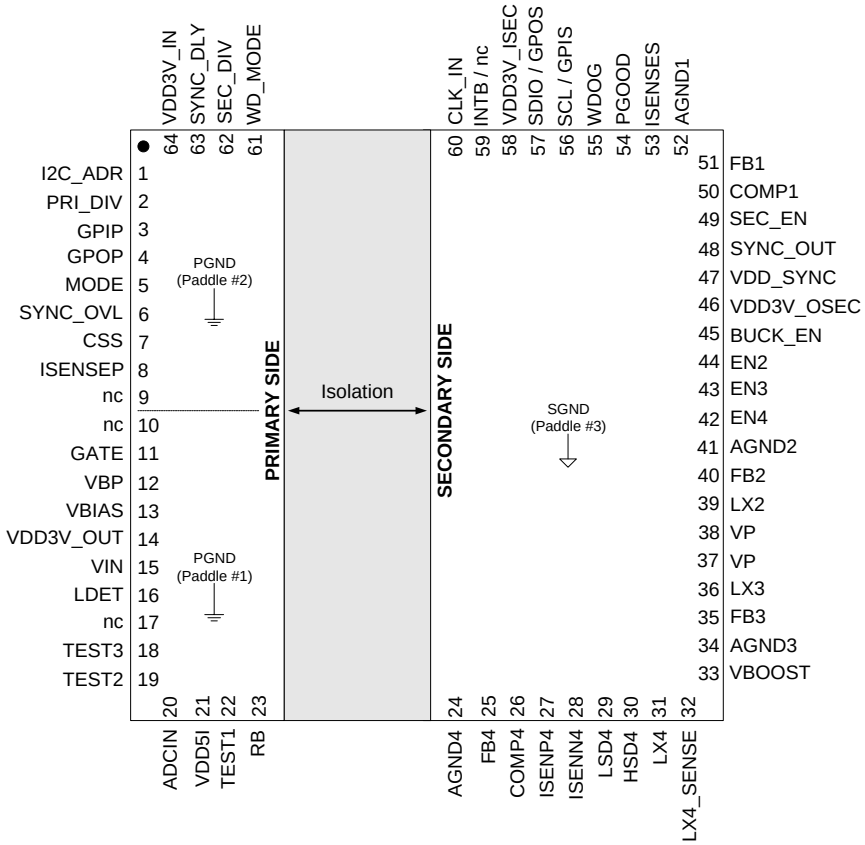


Figure 1 - AS14x4 Pin Diagram

FILTER DESIGN

Input Noise Filter at 48VIN

A pi-type filter should be employed at the input to the 48VIN pin to reduce the amount of noise on the line. The following filter configuration is recommended:

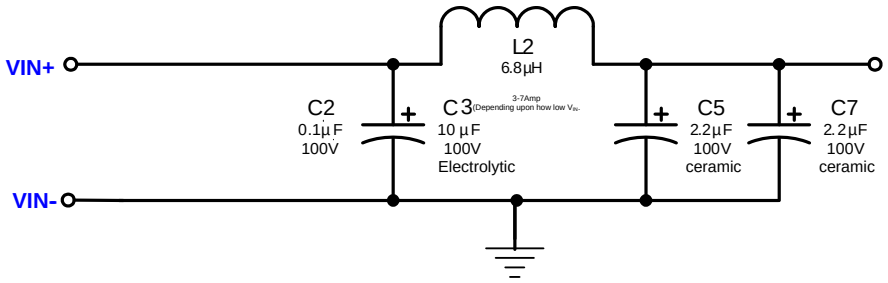


Figure 2 - Pi-Type Filter

In addition, designers must ensure that any device connected to 48VIN be rated to safely handle at least 100V. Component ratings need to be observed carefully in light of ground references. Selection of the the input ceramic capacitor dielectric must take the voltage coefficient into consideration. The values shown are effective capacitance.

SYSTEM PROTECTION FEATURES

The AS14x4 IC has built-in protection features for over-current, over-voltage, and over-temperature fault conditions. Please refer to the product datasheet for detailed information.

For the integrated buck regulator outputs (Vout2 and Vout3), additional external short circuit protection can be implemented by using the following over-current interlock circuit (see Figure 3). This circuit is recommended in particular for applications where both integrated buck regulators are known to be running close to their maximum rated currents.

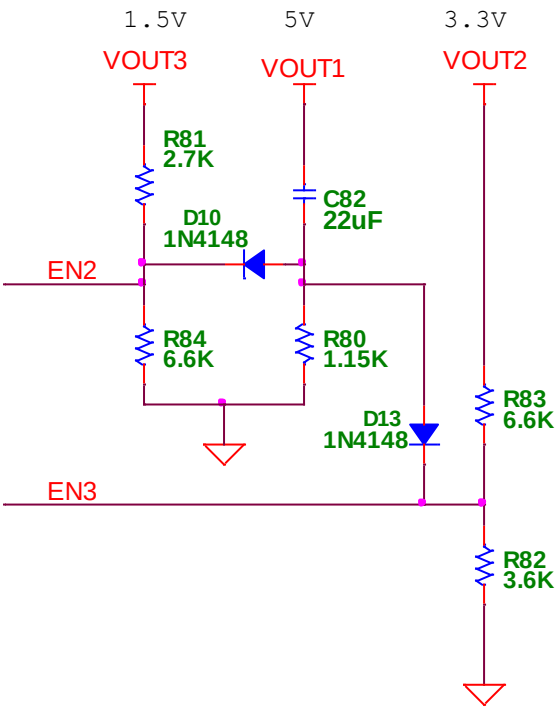


Figure 3 - Buck Regulator Over-Current Interlock Circuit Protection

When the voltage on either buck regulator output drops below a pre-set threshold due to an over-current condition, the enable pins are pulled down to disable both outputs. As designed above, the voltage dividers are set for ~1.1V at the enable pins, and the sum of the two resistors is roughly 10K. The actual threshold chosen for the voltage at the enable pin depends on the sensitivity preferred. The closer the threshold value is set to 0.8V, the more sensitive the circuit is to disabling the buck regulators for a sub-nominal output. For example, the circuit can be made more sensitive for Vout3=1.5V by setting the threshold to 1.05V compared to the 1.15V threshold used for Vout2=3.3V. The associated formulas are below:

1.05V*(R81+R84)/R84 = Vout3; R81+R84 = ~10K
1.15V*(R83+R82)/R82 = Vout2; R83+R82 = ~10K

R80 and C82 depend on the board settings, and the associated time constant should be set to ~10X the ramp rate of Vout1.

PRIMARY CONVERTER

The AS14XX can be operated from an input range from9 to57V. Higher input voltages may be accommodated using an external bias circuit on the VIN pin. Both arrangements are shown below.

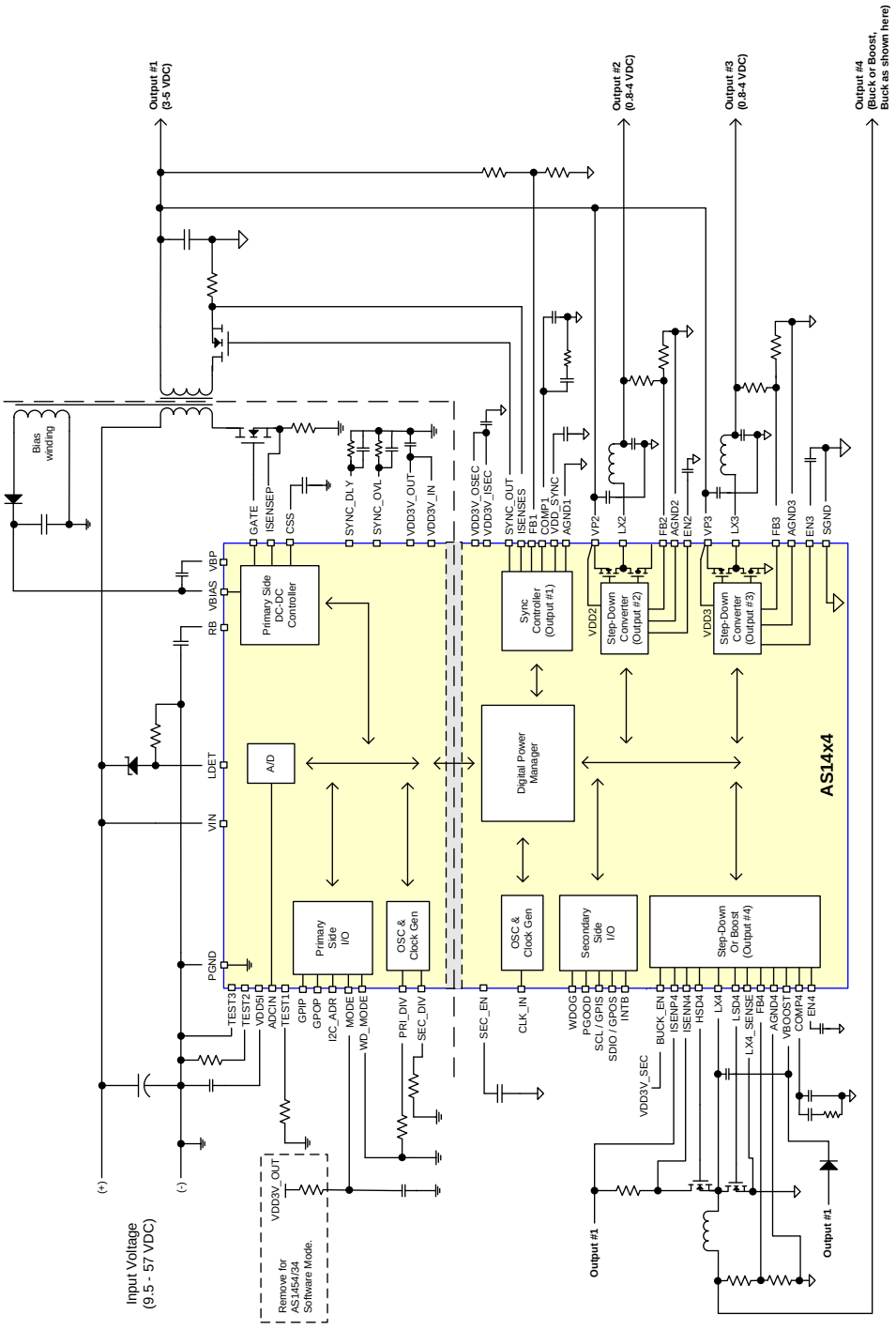


Figure 4 - VIN (max) ≤ 57V

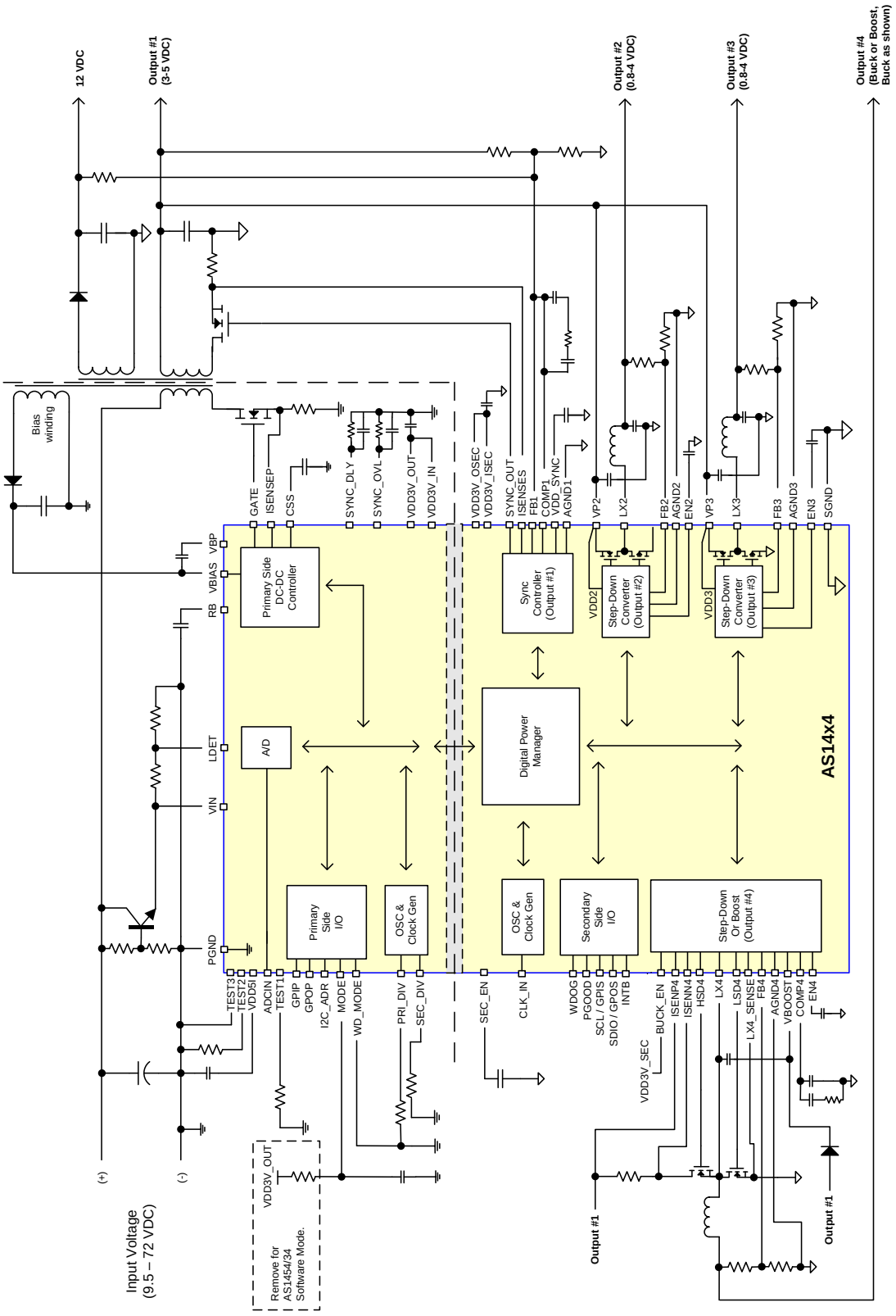


Figure 5 - V_{IN} (max) > 57V

Transformer Selection

There may be many, off-the-shelf transformers that can be used as part of the AS14x4 solution. Such transformers are usually specified in terms of power rating, inductance, turns ratio and output voltage. Selecting the appropriate power rating and output voltage is typically a straightforward process. Selecting the appropriate turns ratio and inductance, however, requires a bit more attention.

Because flyback converters deliver power to the secondary side during the off-time of the primary switch, it is recommended to select a turns ratio that does not exceed duty cycles, D, that is < 50% at V_{IN-MIN}, although the AS14x4 can provide duty cycles up to 80%. Maintaining a low duty cycle significantly reduces the ripple current stress on the output capacitors. Applications using with a very wide input voltage range may require a duty cycle >50%.

To determine the primary-to-secondary turns ratio $N_P/N_S=N$ required for a design, please refer to the following equation with D equal to the highest duty cycle desired at the minimum input voltage:

$$N = D \times V_{IN-MIN} / \left[V_{OUT} \times (1-D) \right]$$

For the primary inductance selection, $L_{PRIMARY}$, it is best to select an inductance that produces a current slope +/- 10% of the average primary current ID at V_{INMIN}:

$$I_{D-PRIMARY} = I_{OUT} / \left[(1-D) \times N_S / N_P \right]$$

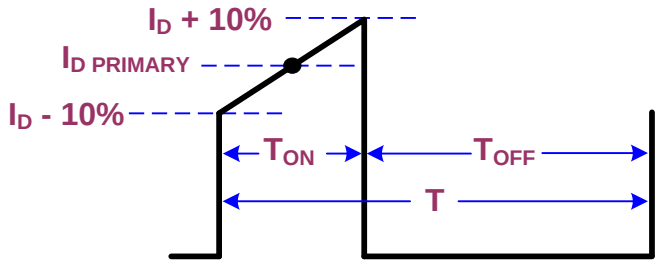


Figure 6 - Duty Cycle and Turns Ratio

$$T_{ON} = 1/F_{SW} \times D \qquad L_{PRIMARY} = V_{IN-MIN} \times T_{ON} / (ID \times 0.2)$$

Although the AS14x4 system still requires an auxiliary winding on the primary side of the transformer for a bias voltage in the range of 8-12V, there is no need for an extra secondary-side gate-drive winding for the synchronous FET because the integrated isolation of the AS14x4 allows for a direct, timing-controlled drive on the secondary side.

The nominal switching frequency typically used for the flyback converter falls in the range of 200kHz to 350kHz, optimizing across various system-design targets such as size, transient response, and efficiency. For a design aiming to achieve the smallest size or the highest efficiency, however, the switching frequency can be pushed toward the ends of the 100kHz-500kHz range. Higher switching frequencies generally result in smaller filter components, while lower switching frequencies tend to yield better efficiencies due to reduced switching losses and core losses.

In terms of power ratings vs. core size, Table 1 below provides general guidance on the relative power capabilities for a range of transformer core sizes.

Table 1 – Transformer Power Rating vs. Core Size

Input Power (W)	Transformer Core Type					
	EP10	EP13	EFD15	EFD20	EFD25	EFD30
15		X	X			
25				X		
30				X	X	
50					X	X

Power/Current carrying capacity of magnetic cores is a strong function of temperature and current. Output power information should be used in conjunction with additional requirements like input voltage range (primary current for fixed power) and temperature for final transformer size selection. EP or EFD designators are for core geometry. External package sizes may vary slightly from manufacturer to manufacturer (e.g. 8-pin vs. 10-pin vs. 12-pin, SMT vs THT). Data is provided here for relative assessment.

Generally, EP-style cores provide very good magnetic coupling in a compact space (taller but less board area), and the cost is moderate. In contrast, EFD-style cores tend to be lower in profile with high effective area (Ae), enabling more room on the bobbin for extra windings, good magnetic coupling, and good shielding. The cost can range from moderate to high.

Prior to designing, please contact Kinetic Technologies for the most recent list of optimized and qualified transformers.

- Coilcraft
  http://www.coilcraft.com
- Halo Electronics
  http://www.haloelectronics.com
- Pulse Engineering
  http://www.pulseeng.com
- Würth Elektronik Group
  http://www.we-online.com

Timing Optimization on Primary Converter

One of the key advantages of the AS14x4 product is that it spans the isolation barrier enabling precise timing control of both the primary-side FET and the secondary-side sync FET. The incorporation of an Overlap/Delay adjust feature allows for the timing relationship to be adjusted by means of two external resistors (see Figure 7). In a conventional system where the secondary-side synchronous FET is driven from an extra "sync" winding on the secondary side of the flyback transformer, parasitic components and tolerances lead to imprecise timing with either excessively long dead times or shoot-through currents. By eliminating such system-design penalties, the designer is enabled to select from a wider range of FETs and still optimize for a specific set of operating conditions.

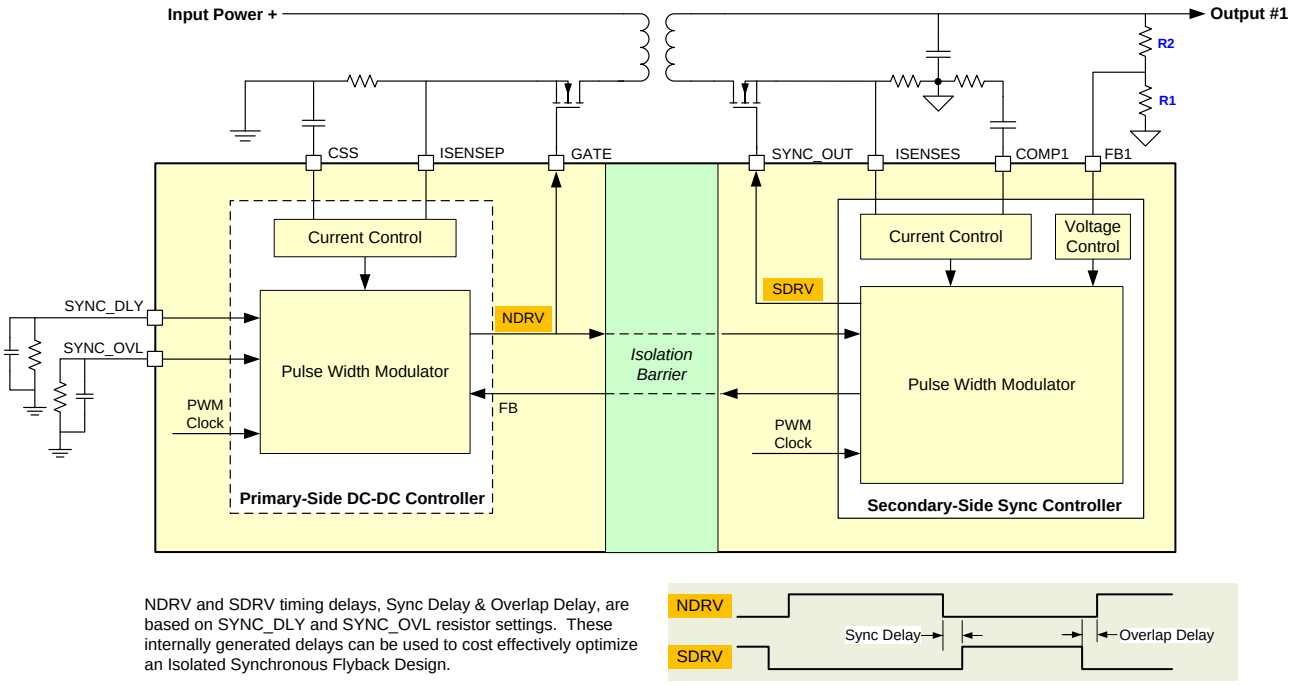


Figure 7 - Converter Timing Control

To understand the timing relationships, it is useful to define the terminology. "Overlap" occurs when both the primary FET and Sync FET are closed at the same time. "Dead-time" occurs when both the primary FET and Sync FET are open at the same time. FET turn-on and turn-off times are also factors that affect the timing between primary and secondary switch nodes.

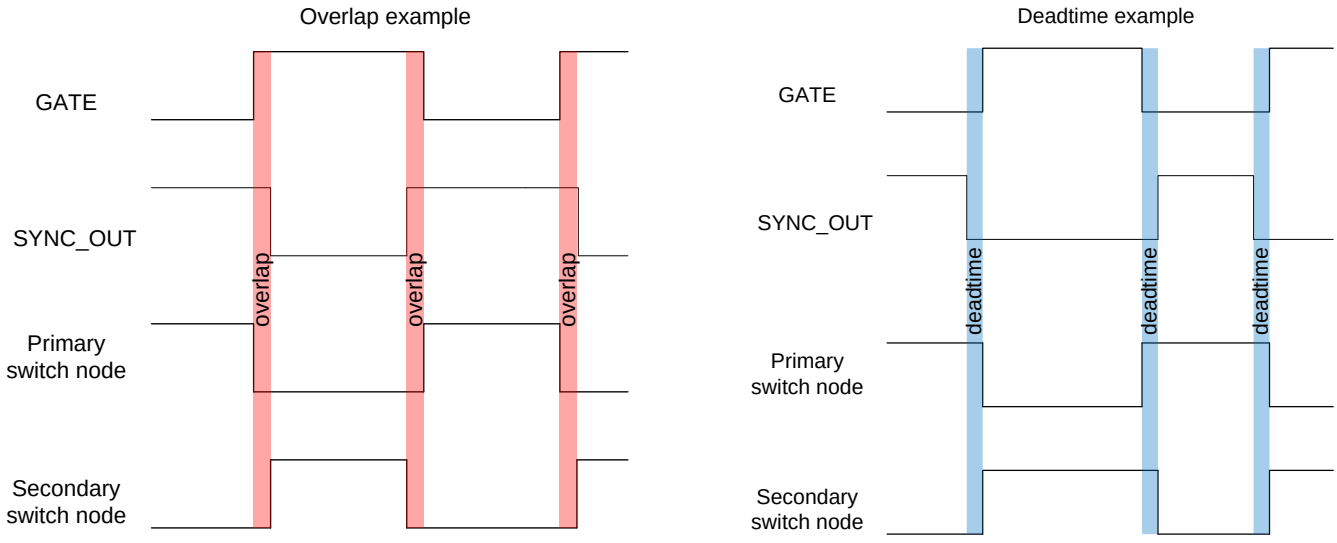


Figure 8 - Overlap and Dead-time Examples

Overlap and dead times can be adjusted using by adjusting "Sync_Dly" and "Sync_Ovl" timing by programming the AS14x4 SYNC_DLY and SYNC_OVL pins.

"Sync_Dly" is used to adjust the delay between the primary GATE signal and the secondary SYNC_OUT signal. Adjusting "Sync_Dly" shifts the entire SYNC_OUT pulse relative to GATE. "Sync_Dly" is adjusted by changing the value of an external resistor. A larger resistor value shifts the delay to the right; a smaller resistor value, to the left.

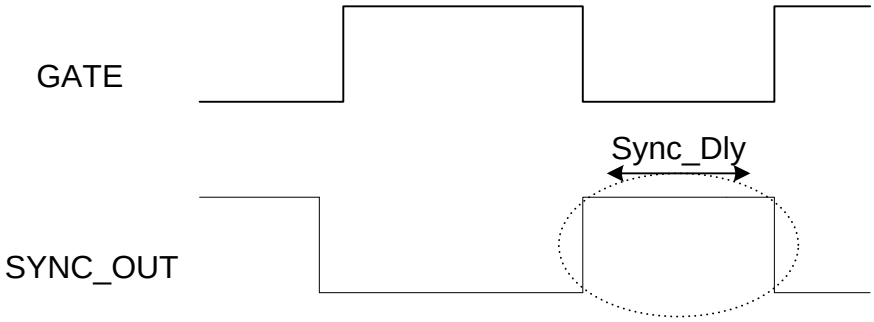


Figure 9 - Sync_Dly Adjustment

Similarly, "Sync_Ovl" is used to adjust the time between the falling edge of SYNC_OUT and the rising edge of GATE. Like "Sync_Dly", "Sync_Ovl is adjusted by changing the value of an external resistor.

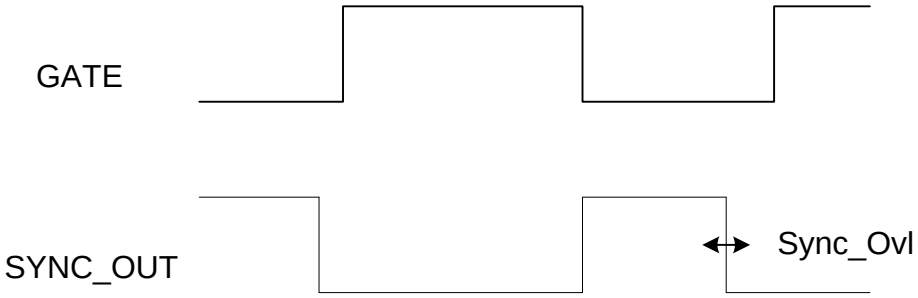


Figure 10 - Sync_Ovl Adjustment

To tune the primary converter timing, the following methodology can be followed. The goal is to ensure that no overlap occurs and to minimize dead-time.

To establish a baseline for the timing, first provide a load to the primary converter and ensure it is running in continuous mode. The output current should be ~2A. Typical converter waveforms can be seen in Figure 11.

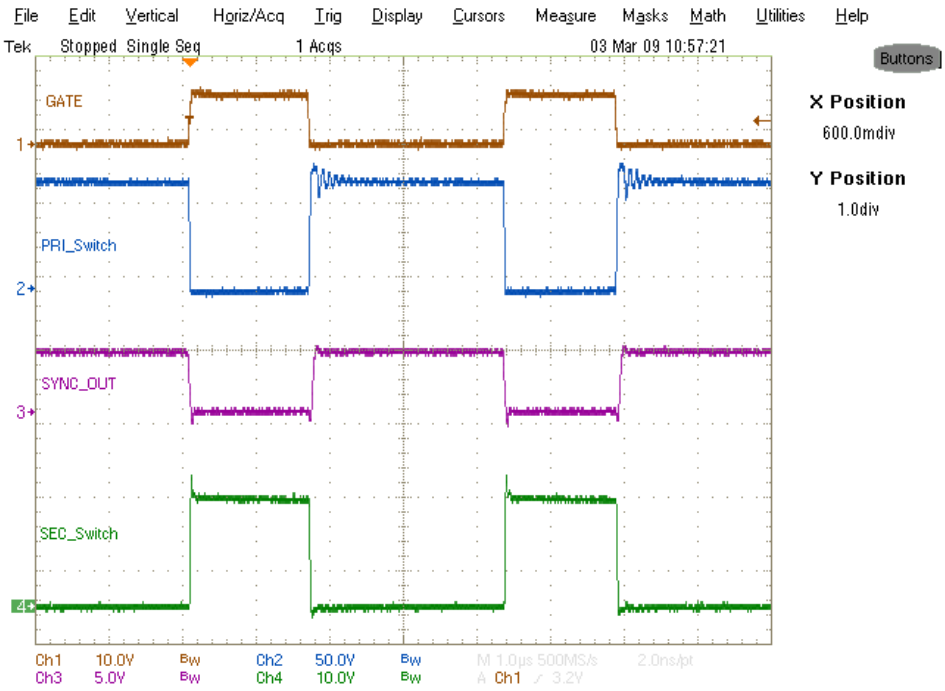


Figure 11 - Typical Waveforms for the Primary Converter

Start by adjusting the "Sync_Dly" resistor so that no overlap occurs at the transition point where the primary FET opens and the synchronous FET closes.

The screen shot in Figure 12 shows the case where overlap is NOT occurring. This is the target behavior.

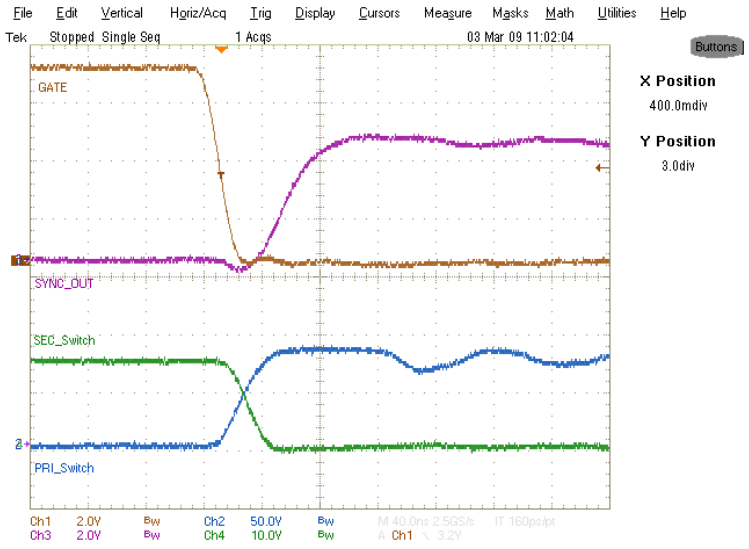


Figure 12 - Target Behavior with No Overlap ("Sync_Dly" adjustment)

In contrast, the screen shot shown in Figure 13 shows a case where overlap is occurring.

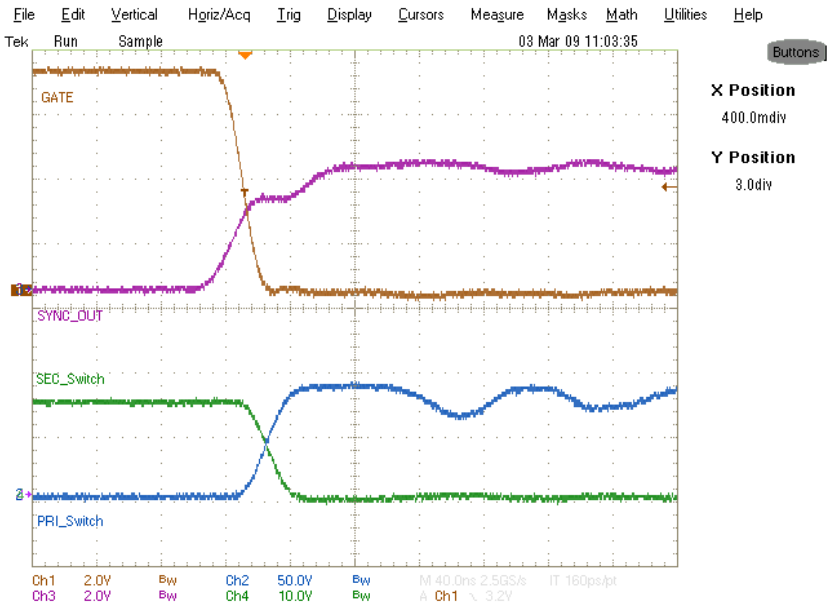


Figure 13 - Example Showing Undesirable Overlap ("Sync_Dly" adjustment)

Then adjust the "Sync_Ovl" resistor so that no overlap occurs at the transition point where the synchronous FET opens and the Primary FET closes. The target waveform is shown in Figure 14.

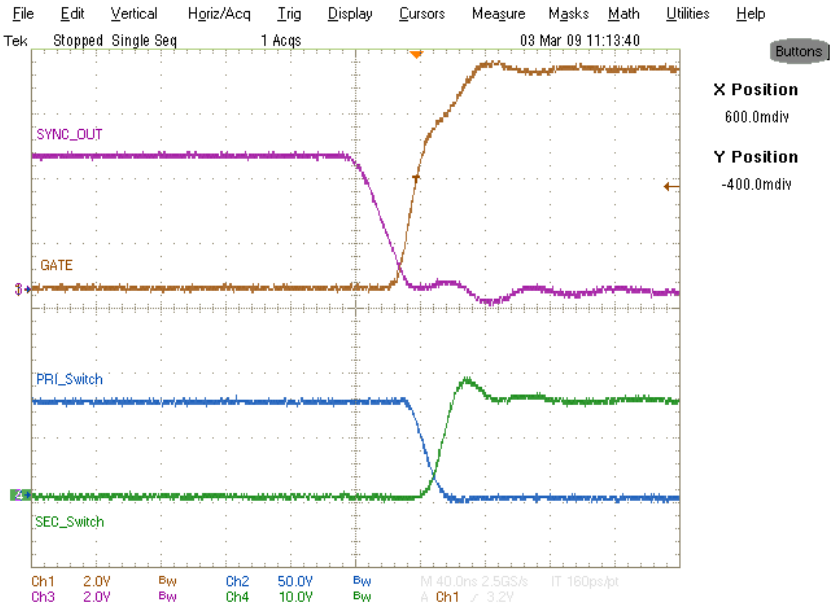


Figure 14 - Target Behavior with No Overlap ("Sync_Ovl" adjustment)

Finally, the two plots in Figure 15 show examples of overlap and dead time in cases where the "Sync_Ovl" adjustment is not optimized.

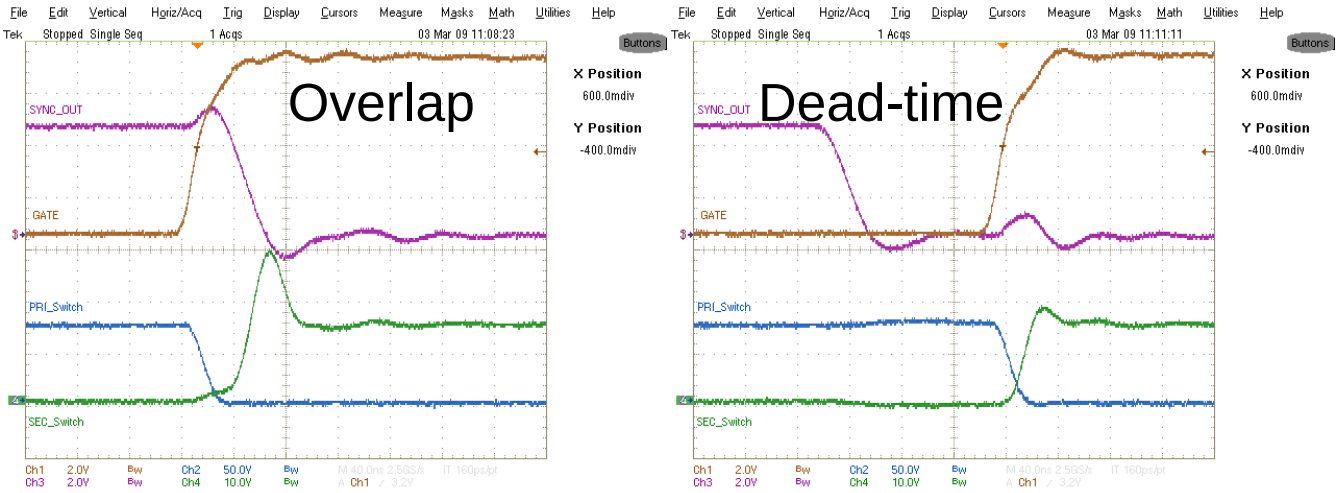


Figure 15 - Examples of Overlap and Dead Time ("Sync_Ovl" adjustment)

The required resistors at SYNC_DLY and SYNC_OVL thus depend on the user's choices for the primary-side and secondary-side NMOS power FETs. The filter capacitors to SGND for these pins are typically 1nF.

MOSFET Selection

FET selection should focus on reducing losses and improving efficiency. Below are details on how to choose the appropriate FETs for use with the AS14x4.

Primary Side

For the primary-side MOSFET selection, there are several criteria to be considered: V_{DS}, V_{GS}, RDS_{ON}, rise/fall times, gate charge, and I_D rating.

V_{DS} is the drain-to-source voltage rating of the FET, and a quick way to determine what the minimum V_{DS} rating should be is to use the following simple formula:

$$V_{DS} = \left[V_{IN-MAX} + \left(V_{OUT} \times N_P / N_S\right)\right] \times 1.5$$

After calculating for V_{DS}, select a FET V_{DS} that meets or exceeds that number under the absolute maximum rating table, keeping in mind that the higher V_{DS} rating usually results in higher drain capacitance which can result in undesired $CV^2/2$ losses. As such, it is not recommended to select a FET that greatly exceeds the calculated V_{DS} above. As a typical example, a FET with a V_{DS} rating of 150V-200V is chosen.

For the gate-to-source voltage V_{GS}, a FET with a minimum V_{GS} of 5V should be used. The gate drive voltage of the AS14x4 should be in the range of 7V-12V, depending on the bias winding voltage generated on the flyback transformer. Because the AS14x4 system has the capability to support gate drives > than 5V, a wide selection of FETs can be used to optimize the cost and performance of the system as needed, noting that the RDS_{ON} and transition time can be greatly influenced by the V_{GS} voltage applied.

RDS_{ON} is the static ON resistance, and I_D is the drain current rating of the selected FET; these two parameters are usually inversely proportional (i.e. the higher the current rating, the lower the RDS_{ON} of the FET).

The main three operating factors in determining the effective RDS_{ON} of a particular FET are the V_{GS} or gate-drive voltage, the drain current, and the junction temperature. The relationship between RDS_{ON} and junction temperature is fairly linear. A simple rule of thumb for RDS_{ON} with respect to junction temperature is that the RDS_{ON} will increase by a factor of 50% from room temperature to 100°C. It is quite reasonable to assume an operating junction temperature of 100°C. In order to decrease dissipation and loss, it is desirable to select a FET with the lowest RDS_{ON} possible; 70 mΩ or less is usually a good number. It is recommended that the RDSon not be greater than 0.15 ohms at 5V V_{GS}. To calculate the drain current (I_D) on the primary FET, first calculate the operating maximum duty cycle:

$$D = (V_{OUT} \times N_P / N_S) / [V_{IN-MIN} + (V_{OUT} \times N_P / N_S)]$$

From the maximum duty cycle, we can then calculate the I_D of the primary FET:

$$I_{D-PRIMARY} = [I_{OUT} / (1-D)] \times (N_S / N_P) \times 1.25$$

Although $I_{D\text{-}PRIMARY}$ is not a continuous-drain current, one should select a FET that meets or exceeds this rating for continuous-drain current. As a typical example, a FET with an I_D rating of 3A continuous is used.

When picking a FET, attention should also be put on the transition (rise/fall) times, as slow transition times can greatly reduce efficiency. When reviewing datasheets for these FETs, the designer should note that these numbers can greatly depend on the operating conditions of the design. Typically, it is recommended that the rise times (including Ton delays) be faster than 50ns. Similarly, the fall times (including Toff delays) should be faster than 50ns.

Regarding the gate charge, it should not exceed 35nC.

Secondary Side (Synchronous FET)

Like the primary side, the secondary-side synchronous FET selection has V_{DS}, V_{GS}, RDS_{ON}, rise/fall times, gate charge, and I_D as main criteria. To determine the drain current of the secondary side, the average I_D calculated above can be used with a turns ratio scaling factor of N_P/N_S:

$$I_{D-SECONDARY} = I_{D-PRIMARY} \times (N_P / N_S) \times (D / (1-D))$$

This formula implies that the secondary current may be many times greater than the primary current. Thus, a low RDS_{ON} for the secondary FET is even more critical in determining system efficiency. Choose FETs with 10mΩ or less RDS_{ON} (at a V_{GS}=4.5V) in order to reap the benefits of a synchronous design. Typically, for a 15W Flyback design, design for a continuous I_D = 10A; for a 50W Flyback design, design for a continuous I_D = 30A.

To determine the drain to source voltage rating of the selected synchronous FET, we can use the following formula:

$$V_{DS-SYNC} = [V_{OUT} + (V_{IN-MAX} \times N_S / N_P)] \times 1.5$$

Typically, we choose a synchronous FET with V_{DS} = 30V, or 40V if expecting duty cycles <25% on the primary. . In some cases a higher voltage rating may be required depending on the recovery characteristics of the parasitic body diode.

The gate drive voltage provided by the AS14x4 to the sync FET is ~4.8V; it is thus strongly recommended that the V_{GS} threshold for the sync FET be 2.5V or less.

In terms of FET speed, slower turn on times are actually acceptable, with a maximum turn-on time of 150ns. However, a short turn-off time is critically important to prevent possible cross-conduction (shoot-through) with the primary FET. Finally, the maximum recommended gate charge is 45nC.

Output Voltage Programming

Voltage feedback is provided by the FB1 pin. At FB1, an internal reference of 1V (nominal) is compared to a resistor divided voltage from Output #1. This sets the desired Output #1 voltage level. For example, with the top resistor in the feedback divider designated R2 and the bottom resistor in the feedback divider designated R1, the programmed voltage for Output #1 is equal to Vref times (R1+R2)/R1. So, for R1=5K, R2=20K, and Vref=1V, the output voltage is set to 5V.

Compensation

The AS14x4 primary output (#1) has two basic Compensation and Feedback mechanisms: An Adaptive Slope Compensation and a Primary-Secondary Control Loop Feedback.

The Adaptive Slope Compensation automatically provides an optimized ramp framework for the overall loop performance, there are no user settings required.

For the Primary-Secondary Control Loop the AS14x4 uses an internal transconductance error amplifier whose output compensates the control loop. Internal isolation is automatic and completely user transparent to both compensation and feedback loop setup.

Referring to Figure 16, through the COMP1 pin, an additional zero Z1 and pole P1 may be optionally employed for added phase margin and to cancel high-frequency noise, if required. The COMP1 pin is connected to an external RC loop compensation network allowing flexibility to optimize the system performance while insuring loop stability. The extra pole and zero are formed from capacitors C25 and C28 and resistor R29 (per Figure 16).

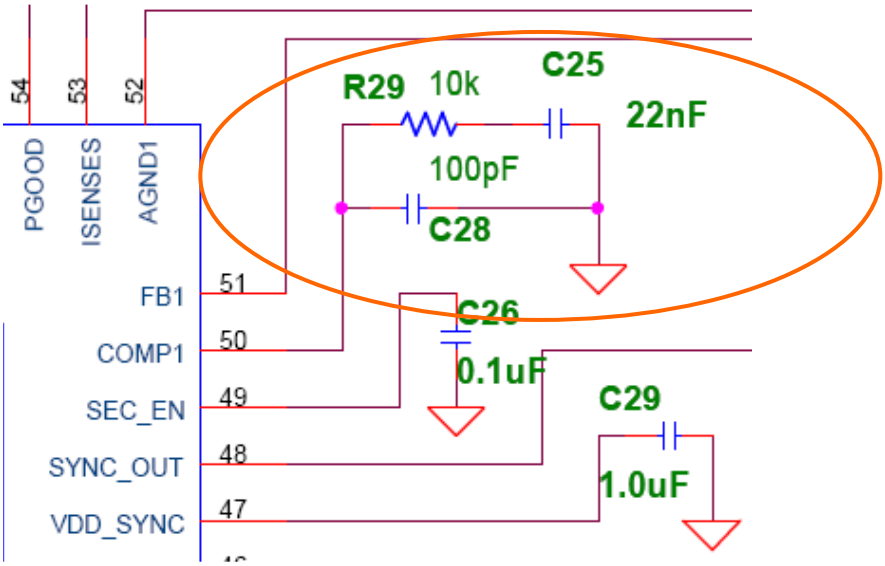


Figure 16 - Primary Converter Compensation Network

The additional pole and zero are calculated using:

$$f_{P1} = \frac{1}{(2\pi \bullet C28 \bullet R29)} \qquad f_{z1} = \frac{1}{(2\pi \bullet C25 \bullet R29)}$$

Selecting appropriate component values for pole and zero positions is the key to achieving the desired high DC gain, phase margin, gain margin, and gain crossover frequency that are the hallmark of a stable system. Typically, the gain-crossover frequency should be less than one-sixth of the switching frequency (F_{SW}).

The optional zero Z1 and pole P1 can be implemented if the system still requires additional phase margin and/or higher DC gain for better load regulation. When the zero associated with the output capacitor ESR (Equivalent Series Resistance) is less than one half of F_{SW}, this additional pole and zero can be used to compensate for or minimize the effect caused by the ESR. Zero Z1 should be set farther out at 10*P2, where P2 is the pole from Cout and Rload. Pole P1 should be set equal to the zero of the ESR (ZESR), using the calculation:

$$f_{ZESR} = \frac{1}{(2\pi \bullet C_{OUT} \bullet R_{ESR})}$$

One further issue designers should pay attention to in flyback designs is the Right Half Plane Zero (RHPZ), which can be found using the following formula:

$$Z_{RHP} = \frac{R_L \bullet (1-D)^2 \bullet N^2}{(2\pi \bullet L_P \bullet D)}$$

where:

- RL is the load resistor
- D is the duty cycle.
- N is the turn ratio of primary to secondary
- LP is the primary inductance of the transformer.

To minimize the effect of the Right Half Plane Zero, the gain-crossover frequency FC should be also set to less than one-third of the RHPZ frequency.

An additional output-filter inductor may be employed, depending on the design's output ripple and load transient response requirements. Use of this inductor changes the impedance of the load seen by the DC-DC control loop and requires appropriate adjustments to the compensation-loop components. Also, if applications require output capacitance different from that specified in the Kinetic reference designs, the loop compensation is affected and appropriate component adjustments will be required, using the preceding design guidelines.

Loop stability testing to generate Bode plots can be performed with a traditional small-signal test setup. Transient load-step response should also be checked, to ensure that the transient behavior matches the measured AC-loop parameters.

Please consult with Kinetic' Application Support engineers for further assistance and proper component selection.

Snubbing Circuit Design

The most common snubbing circuit is the R/C, which is placed as close as practical across the device being protected. The R/C time constant of the circuit should be small in comparison to the switching period, but long relative to the voltage rise time. The capacitor must be larger than the parasitic capacitance, but as small as possible, to minimize power dissipation through the snubbing resistor.

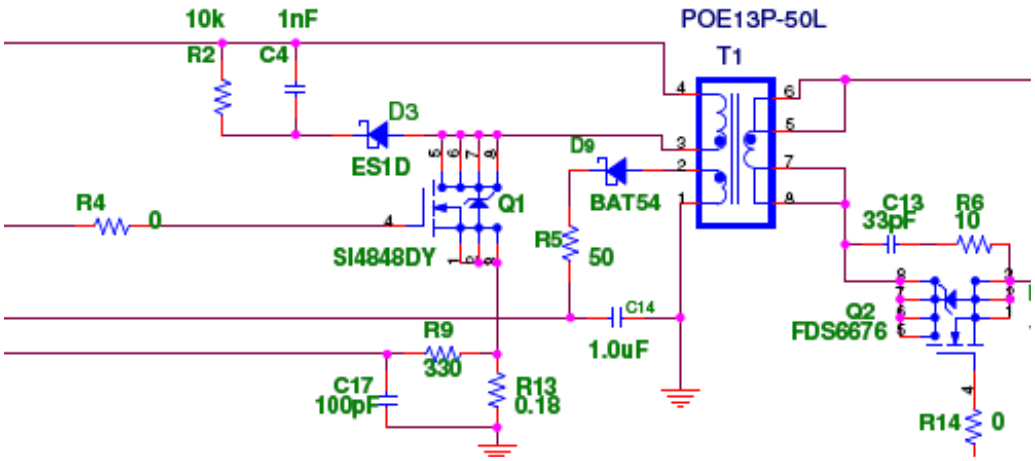


Figure 17 - Snubbing Circuits Used on the AS14x4-CVB15 Design

There are two snubbing circuits used in the AS14x4 reference design shown in Figure 17. The snubbing circuit for the primary-side FET (Q1) consists of R2, C4, and D3. The snubbing circuit for the secondary-side synchronous FET (Q2) is comprised of R6 and C13.

In designing an AS14x4 snubbing circuit, designers should begin by measuring the frequency of the ring without the snubbing circuit in place and then begin tuning the circuit by adding a small capacitor (in the 100pF range) across the device and again observing the ring. Then, increase the capacitance until the ring is roughly halved and note the capacitor value. Finally, for the actual capacitor in the design, select one with 75% of the capacitance value just determined.

Add a 25ohm resistor in series with this capacitor and increase/decrease the resistance until the ring is nearly eliminated. Capacitors should be the ceramic type, which have low ESR and ESL properties. Lossy dielectric ceramic capacitors should be avoided. Use X7R dielectric or better. Avoid wire-wound resistors, which have excessively high ESL.

For the AS14x4, although a synchronous FET is employed, there is no need for an extra synchronous winding in the flyback transformer design! The integrated isolation allows the AS14x4 to drive the gate of the synchronous FET directly.

Adding a snubbing circuit to minimize spikes and ringing can be beneficial for device protection and EMI, but one undesirable effect is a slower switching time, which impacts efficiency. Care must be taken in selecting these components and observing the effects. Board layout plays a significant role in circuit performance, along with transformer parasitic components.

Besides the snubbing circuits in the AS14x4 reference design, various EMI suppression techniques are implemented as alternate solutions whenever needed. For example:

- Resistor R4 can be used to slow down the rising edge of the primary-switching FET.
- Resistor R14 can be used to slow down the rising edge of the synchronous FET.

SECONDARY-SIDE REGULATORS

Power Output Sequencing

The secondary-side regulators can be sequenced as desired by connecting a grounded external capacitor to the respective ENx pins, establishing the desired turn-on delays for each corresponding power output. Each power output delay capacitor can be selected per the following formula to create a user defined power-on sequence.

The time delay (TD) in seconds for a capacitor (Cx) is defined by the formula:

$$TD = \frac{0.8Cx}{10\mu A} \quad \text{(must be > 8ms)}$$

For example, a 200nF cap creates an output delay of 16ms. Each ENx pin has an internal 0.8V threshold detector and sources 10µA. When the ENx pin reaches 0.8V, the power output is turned on. Thus, the delay of the voltage rising to 0.8V through the linear current feeding the external capacitor sets the output delay. Each ENx delay must be greater than 8mS for proper device startup assuming a typical 10nF capacitor on SEC_EN.

All delays for power outputs #2-#4 are synchronized to the beginning of Output #1 voltage ramp (see Figure 18).

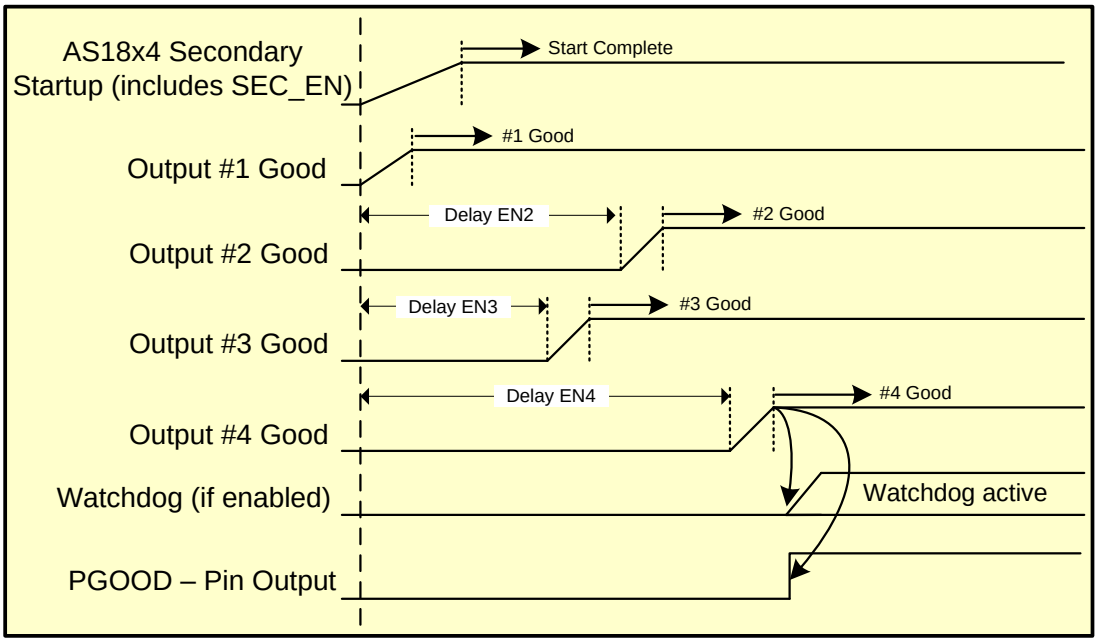


Figure 18 - Power Output Sequencing Example

OUTPUTS 2 AND 3: INTEGRATED BUCK REGULATORS

The AS14x4 includes two integrated 2A buck regulators that feed off the isolated output of the flyback regulator. These two integrated buck regulators are identical; both use current-mode control, are internally compensated, and can deliver up to 2A each. However, due to thermal limitations the total current from both outputs may not exceed 3A. After determining the desired switching frequency F_{SW} for these regulators, one can select the appropriate value inductor by using the following formula:

$$L = V_{OUT} \times (V_{IN} - V_{OUT}) / (V_{IN} \times I_{RPL} \times F_{SW})$$

IRPL is the inductor ripple current, and it is usually recommended to be +/- 30% of the max load current but can typically vary anywhere from +/- 20% to +/- 40%. Typical inductor values for the AS14x4 buck regulators are in the range of 680nH to 3.3uH for a switching frequency of 1MHz. Depending on the switching frequency (from 500kHz to 2MHz), inductor values will shift as well.

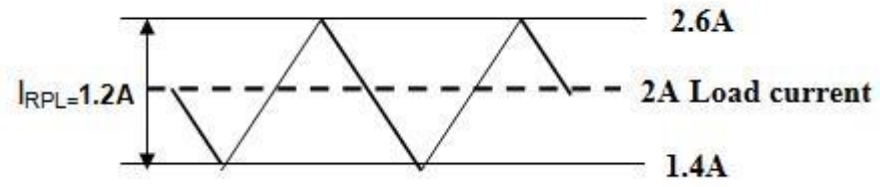


Figure 19 - Inductor Ripple Current

To provide adequate margin and to minimize losses, the saturation current rating for the inductor should be 1.5x higher than the peak inductor current. For the case represented in Figure 19, an inductor with an Isat rating of at least 3.9A is recommended. It is important to factor in the temperature de-rating for the saturation current, as inductors tend to saturate earlier at higher temperatures.

Output Voltage Programming

Voltage feedback is provided by the FB2/FB3 pins. At FB2/FB3, an internal reference of 0.8V (nominal) is compared to a resistor divided voltage from Output #2/#3. This sets the desired output voltage level. For example, with the top resistor in the feedback divider designated R2 and the bottom resistor in the feedback divider designated R1, the programmed voltage for Output #2/#3 is equal to Vref times (R1+R2)/R1. So, for R1=604, R2=1.91K, and Vref=0.8V, the output voltage is set to 3.3V. If the feedback divider resistor values are too large, they can destabilize the loop, so it is recommended that the values not exceed 10K.

Switching-node Snubber

To minimize switching noise on the buck regulators, an RC snubber network (Figure 20) is required from each LX switching node to the VP supply node. The connections for this snubber should be placed as near the IC pins as possible to minimize parasitic component effects. The recommended values are 4.7ohms for the series resistor and 1nF for the series capacitor.

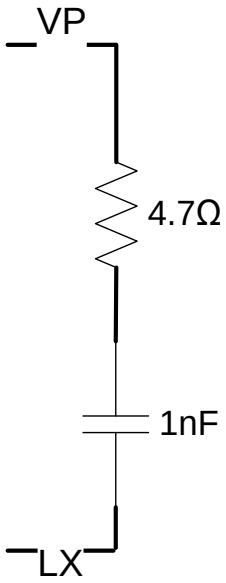


Figure 20 - Buck Regulator Switching-node Snubber

Loop Compensation

Loop compensation is integrated for both outputs, so no external RC loop compensation networks are needed. If additional phase margin and/or bandwidth is desired, however, the FB2/FB3 pull-up capacitor (C1) in Figure 21 provides an important knob for loop stability adjustment.

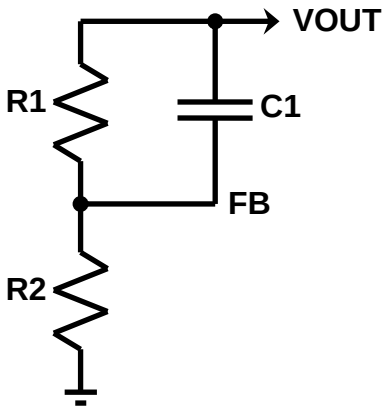


Figure 21 - Buck Regulator Compensation Network

With the addition of the "speed-up" capacitor C1 in the feedback divider, the following pole-zero pair is introduced:

POLE: $f_P = \frac{1}{(2\pi \bullet C1 \bullet R1 || R2)}$ ZERO: $f_Z = \frac{1}{(2\pi \bullet C1 \bullet R1)}$

As an example, consider the present CVB13.R2 BOM (1.5V output), with the following component values: R1 = 1.00K; R2 = 1.15K; C1 = 2.2nF. In this case, the pole = 135kHz, and the zero = 72.3kHz. The target is to place the zero/pole pair just above the 0dB crossover.

For output voltages from 1-2V, size pull-up capacitors for a zero roughly equal to 2000/(pi*sqrt(Cout)). For example, with Cout=2*47uF, the target zero frequency is 65.7kHz.
For a 3.3V output and Cout=2*47uF (with a loop bandwidth around 35kHz), size the pull-up capacitor for a zero around 40-45kHz.

After implementing any adjustments to the buck loop compensation, it is important to verify stability by either looking at loop gain/phase measurements (i.e. Bode plots) or examining the step response behavior to see if there is excessive ringing or other signs of instability.

Output Capacitance

The maximum capacitance is bounded by the need to limit the startup current. Specifically, Cout,max is given as the following:

$$C_{out,max} = (500/(V_{out}*f_{buck}))*(2A - I_{load,ss})$$

where fbuck is the buck switching frequency, and Iload,ss is any additional current drawn by the load during startup. The minimum capacitance is bounded by the maximum closed-loop bandwidth of 100kHz and is set by the following:

$$C_{out,min} = 225e\text{-}6/(\pi * V_{out})$$

As a general rule of thumb: 40uF to 400uF serves as a good range for output capacitance; the nominal recommendation is 2x47uF MLCCs per rail.

VOUT4: BUCK CONFIGURATION

In addition to the two integrated buck regulators that feed off the isolated output of the flyback regulator, the AS18x4 also supports a fourth DC/DC output with an integrated controller that can be configured to operate as either a buck or a boost converter, utilizing external FETs for power-rating flexibility. Boost or buck operation is selected by the BUCK_EN pin. BUCK_EN=VOUT1 will ensure buck mode operation.

Theory of Operation

For typical buck operation (Figure 22), the converter uses an output from the PWM comparator and generates driver signals for both high-side and low-side MOSFETs. To produce these PWM loop-corrected outputs, an error signal from the voltage-error amplifier is compared with the ramp signal generated by an oscillator in the PWM.

The external high-side switch is turned on at the beginning of the oscillator cycle and turns off when either the ramp voltage exceeds the internally-generated reference signal or the current-limit threshold is exceeded. The external low-side switch is then turned on until either the end of the cycle or until current reversal occurs.

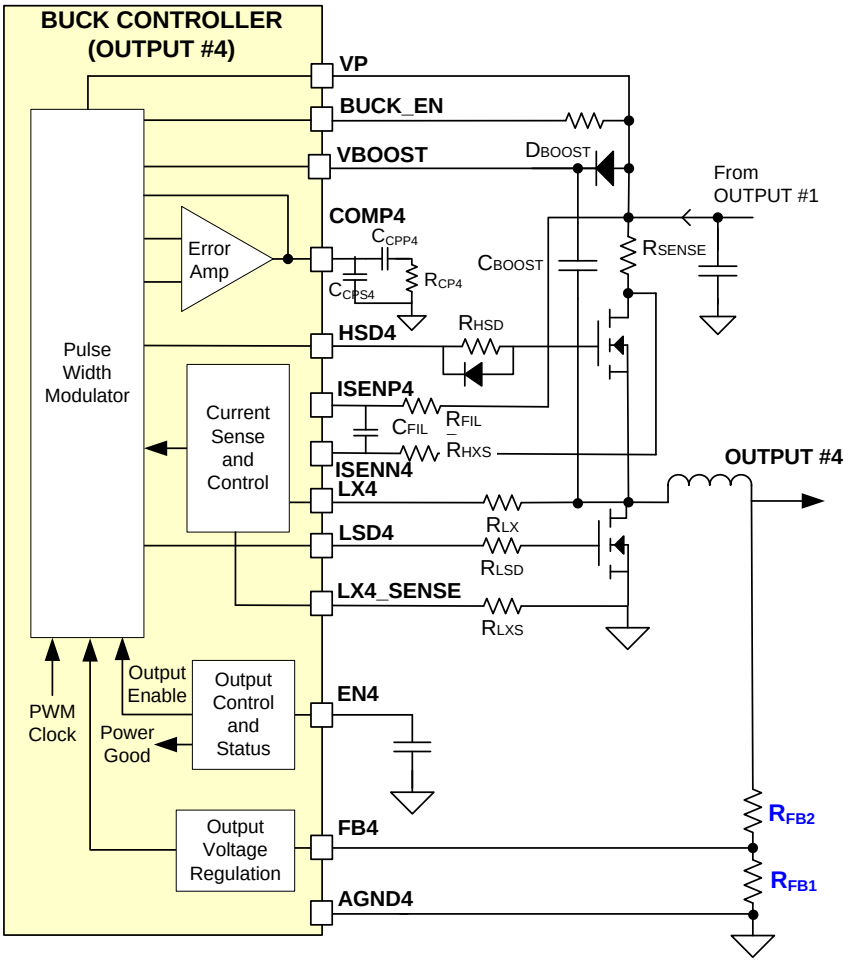


Figure 22 – Output #4 as Buck – Block Diagram

Gate Drive Operation

In order to use inexpensive NMOS power FETs, the HSD4 driver is bootstrapped to approximately twice the VP supply voltage when turned on. Proper connection of the V_{BOOST} diode and capacitor is necessary for proper operation.

In order to ensure smooth bootstrap operation, resistors R_{LX} and R_{HSD} must be set to 4ohm and 20ohm, respectively. R_{HXS} and R_{LXS} should equal R_{LX}. Failure to add these components can lead to erratic gate-drive operation, including the LSD4 signal not turning on. The parallel diode is recommended but not required.

The LSD4 pin is a standard FET driver that swings between VP and ground. In order to maximize efficiency, the LSD4 is self-timed to the LX4 falling edge. The LSD4 signal turns off upon either the end of the conversion cycle, or via the current reversal detection described below. Improper implementation of current-reversal detection can result in runt or short pulses on the LSD4 node.

Current-sense Resistor Selection

The buck can be configured for arbitrary current levels through scaling by proper sense resistor selection. R_{SENSE} should be selected such that I_{PEAK} (defined as I_{AVG} + I_{RIPPLE}) produces a 60mV voltage on this node. For example, in a 4A supply, with a 30% ripple, I_{PEAK}=5.2A and R_{SENSE}=11.5milliohm.

Short circuit is detected when the voltage on R_{SENSE} is greater than 90mV. Use of too large of a sense resistor may result in supply shutdown during normal operation. Using too small of a sense resistor will result in an efficiency penalty if a 'light load' is declared during full power operation.

ISENP/N4 are differential signals and must be configured as a Kelvin connection in the layout. The filter capacitor must be placed close to the AS1854.

Current Reversal Detection

To optimize light-load efficiency, the secondary FET is disabled when current reversal is detected. This is done by monitoring LX4 and turning off the secondary FET when the voltage is greater than ~10mV.

LX4 and LX4_SENSE are differential signals and must be configured as a Kelvin connection in the layout. Improper layout may result in false current-reversal detection, causing short pulses on the LSD4.

Inductor Selection

The same basic design approach can be used as is employed for the integrated regulators (Output #2 and #3). For a given switching frequency, F_{SW}, the system designer can select the appropriate inductor value by using the following formula:

$$L = V_{OUT} \times (V_{IN} - V_{OUT}) / (V_{IN} \times I_{RPL} \times F_{SW})$$

Again, I_{RPL} is the inductor ripple current and it is usually recommended to be +/- 30% of the max load current.

To provide adequate margin and to minimize losses, the saturation-current rating for the inductor should be 1.5x higher than the peak inductor current. It is important to factor in the temperature de-rating for the saturation current, as inductors tend to saturate earlier at higher temperatures.

VOUT4 is a current-controlled loop and using too small of an inductor can result in poor signal to noise ratio resulting in apparent loop instability.

Output Voltage Programming

Voltage feedback is provided by the FB4 pin. At FB4, an internal reference of 0.8V (nominal) is compared to a resistor-divided voltage from Output #4. This sets the desired output voltage level. For example, with the top resistor in the feedback divider designated R_{FB2} and the bottom resistor in the feedback divider designated R_{FB1}, the programmed voltage for Output #4 is equal to V_{REF} x (R_{FB1}+ R_{FB2})/R_{FB1}. So, for R_{FB1}=604ohm, R_{FB2}=1.91Kohm, and V_{REF}=0.8V, the output voltage is set to 3.3V.

FB4 and AGND4 are differential signals and must be configured as Kelvin connections in the layout.

Loop Compensation

The COMP4 pin is connected to an external R/C loop compensation network, allowing flexibility to optimize the system performance while insuring loop stability. Through the COMP4 pin, an additional zero Z_1 and pole P_1 may be optionally employed for added phase margin and to cancel high-frequency noise, if required. The extra pole and zero are formed from capacitors C_{CPS4} and C_{CPP4} and resistor R_{CP4} (Figure 22).

The additional pole and zero are calculated using:

$$f_{P1} = \frac{1}{(2\pi \times C_{CPS4} \times R_{CP4})}$$

$$f_{Z1} = \frac{1}{(2\pi \times C_{CPP4} \times R_{CP4})}$$

Selecting appropriate component values for pole and zero positions is the key to achieving the desired high DC gain, phase margin, gain margin, and gain crossover frequency that are the hallmark of a stable system. Typically, the gain-crossover frequency should be less than one-sixth of the switching frequency, F_{SW}.
The optional zero Z_1 and pole P_1 can be implemented if the system still requires additional phase margin and/or higher DC gain for better load regulation. When the zero associated with the output capacitor ESR (Equivalent Series Resistance) is less than one half of F_{SW}, this additional pole and zero can be used to compensate for or minimize the effect caused by the ESR. Zero Z_1 should be set farther out at 10 x P_2, where P_2 is the pole from C_{OUT} and R_{LOAD}. Pole P_1 should be set equal to the zero of the ESR (ZESR), using the calculation:

$$f_{ZESR} = \frac{1}{(2\pi \times C_{OUT} \times R_{ESR})}$$

As in the case of VOUT1, we set the closed-loop unity gain bandwidth by setting the compensation resistor, R_C, as follows:

$$R_C = \frac{2\pi \times f_0 \times 6.3 R_{SENSE} \times C_{OUT}}{G_M} \times \left(\frac{V_{OUT}}{V_{REF}}\right)$$

$$G_M = 75\mu s$$

$$f_0 = \tfrac{1}{6} f_{SW}$$

$$V_{REF} = 800mV$$

where f_0 is the desired unity-gain bandwidth, V_{REF} is the feedback voltage reference, and V_{OUT} is the converter output voltage. Typically, f_0 should be set no larger than 1/10 to 1/6 of the converter switching frequency.

The load step response can now be calculated from:

$$\Delta V_{FB} = \frac{\Delta I_{LOAD}}{R_C} \times \frac{6.3 R_{SENSE}}{G_M}$$

Here, ΔI_{LOAD} is the load step, ΔV_{FB} is the allowable feedback-voltage deviation, G_M is the error-amplifier transconductance, and R_{SENSE} is the sense resistance. The factor of 6.3 is included to account for the current-sense gain stage inside the IC.

Next, select the compensation capacitor, C_C, such that the resulting compensation zero frequency, Z_C, is well below the desired unity-gain bandwidth. For example, setting the zero to 1/10 of f_0 is as follows:

$$Z_C = \frac{f_0}{10} = \frac{1}{2\pi \times R_C \times C_C} \Rightarrow C_C = \frac{5}{\pi \times f_0 \times R_C}$$

If the output capacitance has excessive ESR it might create an undesirable zero in the converter loop response. This can be overcome with an additional capacitor, C_{C2}, from the COMP pin to ground, creating a pole in the compensation network:

$$C_{C2} = \frac{R_{ESR}}{R_C} \times C_{OUT}$$

Setting C_{C2} to this value precisely cancels out the ESR zero.

MOSFET Selection

For both the high-side and the low-side FETs used in the fourth-output, buck-regulator configuration, the n-channel FETs chosen should be sized ideally for the target application and load current. When implementing a 4A application, for example, we typically use a FET with a V_{DS} rating of 12V, an I_D rating of 7A or more, and a low RDS_{ON} (e.g. 15milliohm or less RDS_{ON} at a V_{GS}=4.5V). The V_{GS} threshold should be no greater than 2-3V. Rise/fall times should be ~30-50ns or faster, and the gate charge should be ~20nC or so.

VOUT4: Buck Converter – Quick Start

To obtain a preliminary set of system component values, refer to the spreadsheet tool, 'DT080_AS18x4_Design_Tool_vx.y.xls'. This tool will allow the user to quickly determine what component values are needed for a particular system configuration.

VOUT4: VOLTAGE BOOST CONFIGURATION

BUCK_EN=GND will ensure boost mode operation.

Theory of Operation

For typical boost operation (see Figure 23) the converter uses an output from a PWM comparator and generates only a low-side driver signal for a single external MOSFET. To produce this PWM loop-corrected output, an error signal from the voltage-error amplifier is compared with the ramp signal generated by an oscillator in the PWM.

The external low-side switch is turned on at the beginning of the oscillator cycle and turns off when either the ramp voltage exceeds the internally generated reference signal or the current-limit threshold is exceeded. The diode conducts for either the remainder of the cycle or until the inductor current is discharged.

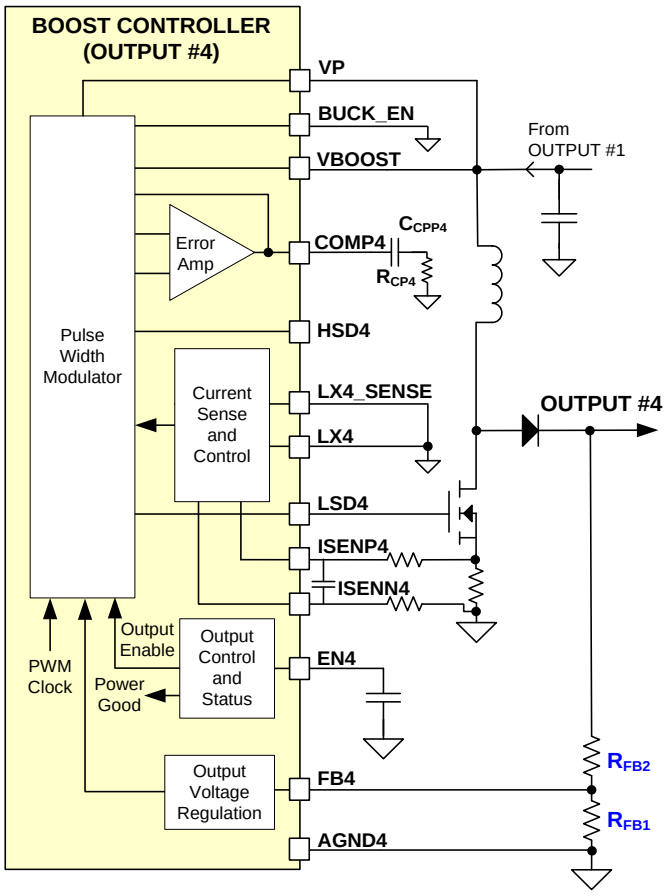


Figure 23 – Output #4 as Boost – Block Diagram

Gate Drive Operation

The HSD4 driver is unused in boost operation and must be left floating. V_{BOOST} must be connected to VP.

The LSD4 pin is a standard FET driver that swings between VP and ground.

Current-sense Resistor Selection

The boost can be configured for arbitrary current levels by scaling by proper sense resistor selection. R_{SENSE} should be selected such it produces a 60mV peak voltage on this node during full power operation. I_{PEAK} is calculated as follows:

$$Duty\_Cycle = \frac{(V_{OUT} - V_{IN})}{V_{OUT}}$$

$$I_{PEAK} = I_{LOAD} \times \left(\frac{1 + ripple}{D}\right)$$

$$R_{SENSE} = \frac{60mV}{I_{PEAK}}$$

For example: With V_{IN} =5V, V_{OUT}=12V/1A supply and ripple=30%, then:

- D = 58.3%
- I_{PEAK} = 1A x (1.3/.583) = 2.23A
- R_{SENSE} = 60mV/I_{PEAK} = 26.9milliohm

Short circuit is detected when the voltage on R_{SENSE} is greater than 90mV. Use of too large of a sense resistor may result in supply shutdown during normal operation. Use of too small of a sense resistor will result in an efficiency penalty if 'light load' is declared during full-power operation.

ISENP/N4 are differential signals and must be configured as Kelvin connections in the layout. The filter capacitor must be placed close to the IC.

Current-reversal Detection

Since the boost is asynchronous, no detection is needed. LX4 and LX4_SENSE should be connected to ground.

Inductor Selection

The same basic design approach can be used as that for the integrated regulators (Outputs #2 and #3). For a given switching frequency F_{SW}, the system designer can select the appropriate value inductor by using the following formula:

$$L = V_{OUT}^{\ 2} \times (V_{IN} - V_{OUT}) / (V_{IN}^{\ 2} \times I_{RPL} \times F_{SW})$$

Again, I_{RPL} is the inductor ripple current and it is usually recommended to be +/- 30% of the max load current. To provide adequate margin and to minimize losses, the saturation current rating for the inductor should be 1.5x higher than the peak inductor current. It is important to factor in the temperature de-rating for the saturation current, as inductors tend to saturate earlier at higher temperatures.

VOUT4 is a current-controlled loop. Using too small of an inductor may result in loop instability.

Output Voltage Programming

Voltage feedback is provided by the FB4 pin. At FB4, an internal reference of 0.8V (nominal) is compared to a resistor-divided voltage from Output #4. This sets the desired output voltage level.

For example, with the top resistor in the feedback divider designated R_{FB2} and the bottom resistor in the feedback divider designated R_{FB1}, the programmed voltage for Output #4 is equal to V_{REF} x (R_{FB1}+ R_{FB2})/ R_{FB1}.

So, for R_{FB1}=100ohms, R_{FB2}=1.4Kohms and V_{REF}=0.8V, the output voltage is set to 12V.

FB4 and AGND4 are differential signals and must be configured as a Kelvin connection in the PWB layout.

Loop Compensation

Design of the loop compensation for Output #4 in boost mode follows that of the buck-mode calculations (noted in the previous section) with the exception that care must be taken to account for the inherent right-half-plane zero of the converter. The RHP zero can be calculated as follows:

$$Z_{RHP} = \frac{R_{LOAD}}{2\pi \times L_{OUT}} \times \left(\frac{V_{IN}}{V_{OUT}} \right)^2$$

As a result, the inherent loop bandwidth must be significantly lower than the RHP zero.

MOSFET Selection

The FET chosen should be sized ideally for the target application and load current. The I_D rating should be 150% greater than I_{PEAK} calculated in the current-sense resistor section, with an RDS_{ON} (e.g. 15milliohm or less at a V_{GS}=4.5V). The V_{GS} threshold should be no greater than 2-3V. Rise/fall times ~30-50ns are generally acceptable, as well as a gate charge of around 20nC. V_{DS_MAX} should be 150% of the output voltage.

FREQUENCY SELECTION

Table 2 – PWM Clock Rate Configuration

AS14x4 Master Clock Rate = Internal, or 25MHz if using CLK_IN		PRI_DIV Resistor (Ω)			
		12.4K	43.2K	68.1K	100.0K
SEC_DIV Resistor (Ω)	VOUT2/3/4 Clock Rate (MHz)	PWM1 Clock Rate (KHz)			
12.4K	2.08/2.08/0.502	reserved	521	417	347
43.2K	1.04/1.04/0.26	347	260	208	174
68.1K	0.69/0.69/0.1725	231	174	139	116
100.0K	0.52/0.52/0.13	174	130	104	reserved

I²C PROGRAMMING

Please refer to the datasheet and "AN092 - AS14x4 Software Users Guide" for detailed guidance on implementation and operation in software mode. A GUI (graphical user interface) program is also available to demonstrate the features accessible through the software interface. Please contact an Kinetic representative for more details.

GENERAL PURPOSE ADC

The ADCIN pin on the Primary side is an input to an internal A/D converter that is read in the A/D Voltage register (08h). The A/D process is automatic so no user action is required to initiate a conversion.

The ADCIN pin interfaces to an internal 8-bit A/D sub-system that contains a successive approximation A/D, track/hold circuitry, internal voltage reference, and conversion clocking. Maximum latency is 10mS (100Hz minimum rate).

In addition, the A/D Alarm Threshold register (09h) allows the user to specify a maximum A/D value that when exceeded automatically sets the A/D Over-threshold Alarm bit in register 00h.

GENERAL PURPOSE I/O

Another benefit of the AS14x4 is that opto-couplers are not required in order to pass signals across the isolation barrier. Opto-couplers are notorious for aging, poor thermal performance, low bandwidth and reducing efficiency.

The GPIO pins provide a means for controlling and monitoring isolated primary side signals from the secondary side of the AS14x4 and are available to the system designer for general use.

The secondary-side GPOS and GPIS pins map to the primary-side pins, GPIP and GPOP, as shown in Figure 24.

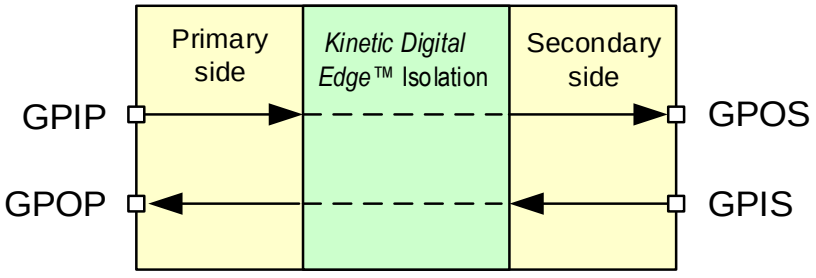


Figure 24 - Inductor Ripple Current

INTRODUCTION TO LAYOUT CONSIDERATIONS

Printed-circuit board layout, stack-up and routing can dramatically affect the performance of a switching regulator design. A poorly designed board can degrade regulator efficiency, noise performance and sometimes even loop stability. At higher switching frequencies, a board's physical characteristics become especially critical. Properly-designed layout, routing, component placement and layer stack-up are vital to a successful FLYBACK implementation with good electro-magnetic (EM) performance.

PWB Layer Stack-Up

It is recommended that a minimum of four (4) board layers be employed in a Flyback design. A six-layer board is preferable, especially when designing with the AS14x4 using all four outputs, because the additional two layers can be used as dedicated, uninterrupted GND planes. A copper plating weight of 1oz is recommended for both the top and bottom layers. Such an approach assists with thermal conduction, EMI emissions, and immunity.

A proper layer stack-up is important for good performance. Always place an uninterrupted GND plane directly underneath any component layer, with ≤ 8mil separation. If the board has double-sided component placement, then GND planes are required on layers 2 and 5 (next to each component layer). Layers 3 and 4 should be used for split power planes and signal traces.

Component Placement

It is highly recommended to place all power-train components in close proximity to one another, especially the transformer, primary FET, snubber circuit(s), sync FET and sense resistors. Traces for these components should be kept as short and wide as possible, to minimize parasitic inductance and resistance. In addition, avoid routing ground-plane fill or signal traces underneath the FLYBACK transformer, this will reduce the amount of transformer noise injected onto the planes and will significantly improve conducted-emission performance by minimizing transformer noise coupling.

Keep the nodes connecting the LX pins to the inductor on the integrated buck-regulators section as close to the AS14x4 as possible. In a discrete buck-controller power-train design, both FETs and the inductor should also be kept close together. In both cases, shielded inductors are always advisable, for better EM performance.

As a general guideline, most buck-regulator output capacitors should be grouped together and placed close to the load. Also, all capacitors experiencing high-RMS currents, such as primary-input capacitors and (especially for the flyback) secondary-output capacitors, must have sufficient numbers of vias to achieve their full, intended influence on circuit performance. Traces carrying high-RMS currents should be routed to accommodate capacitor placement, as shown in Figure 25.

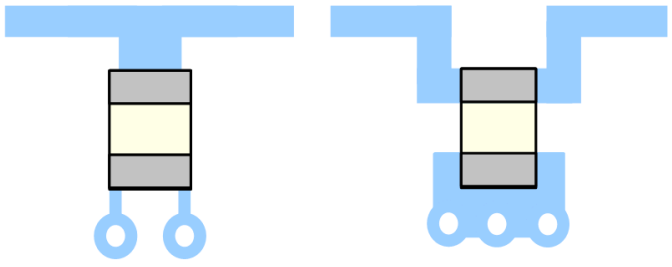


Figure 25 - Noise-Decoupling Capacitor Layout Guideline

All noise-decoupling capacitors on the AS14x4 traces, such as those connected to SYNC_DLY, VBP, VDD3V_OUT, VDD_SYNC and VDD5I, should be located as close as possible to the AS14x4 and on the same layer as the chip. Placing decoupling capacitors on the bottom layer, below the AS14x4, is not as effective, because the associated high-frequency currents circulate through longer return paths, subjecting the bypassing to higher parasitic inductance.

The VP node (input to the buck regulators), in particular, needs to be bypassed carefully by placing the associated ceramic decoupling capacitors as close to the chip pins as possible.

Figure 26 shows an example layout based on Kinetic' evaluation board design:

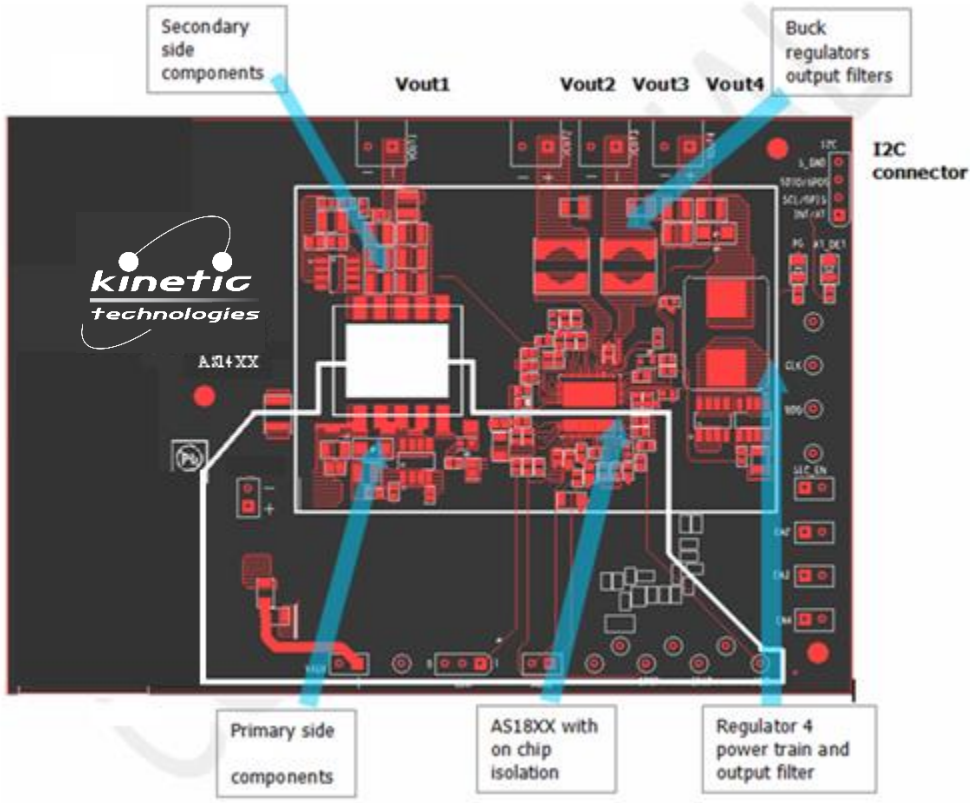


Figure 26 - Component Placement Guidelines

PRIMARY / SECONDARY PWB ISOLATION

The DC-DC converter creates isolated voltages away from the high-voltage signals delivered on the input power lines. Because of this, two independent ground-plane systems must be designed onto the board, one for the high-voltage input side (Primary) and the other for the low-voltage output side (Secondary). This voltage and ground isolation applies to all board layers and components. No traces, pads or vias should be allowed in the isolation gap between the two planes (shown as a solid white line in Figure 26).

At the beginning of the layout process, designers should plan for the minimum 50mil PWB isolation gap between the Primary and Secondary ground planes. Furthermore, it is advised to comply with IPC-2221 PWB spacing guidelines. For improved EM performance, it is advisable that the Primary GND be completely encircled by the Secondary GND, as shown in the split white line in Figure 26. It is recommended, moreover, to clear all copper on all layers from under the transformer.

Note: Designing with the AS14x4 does not require the use of opto-couplers to pass signals across the isolation gap, since the Kinetic AS14x4 Digital Edge™ Isolation technology already provides clean, digital signal communication between the primary and secondary sides.

SENSE LINES AND FEEDBACK DIVIDERS

For Outputs 2, 3 and 4, it is important to note that nodes such as AGND2, 3 and 4 may appear on schematics as GND nets, when in fact they belong to their respective feedback-sense grounds, Do NOT connect these pins directly to their associated ground plane by using a via, as shown of the left side of Figure 27. Instead, connect all feedback resistor dividers directly to the output capacitor pads, rather than to the GND planes (as shown on the right side of Figure 27. Route the sense lines (FB2/AGND2) as a differential pair, in parallel and close proximity to each other. The ground planes can be employed as a shield for these and other sensitive signals, to protect them from capacitive or magnetic coupling of high-frequency noise.

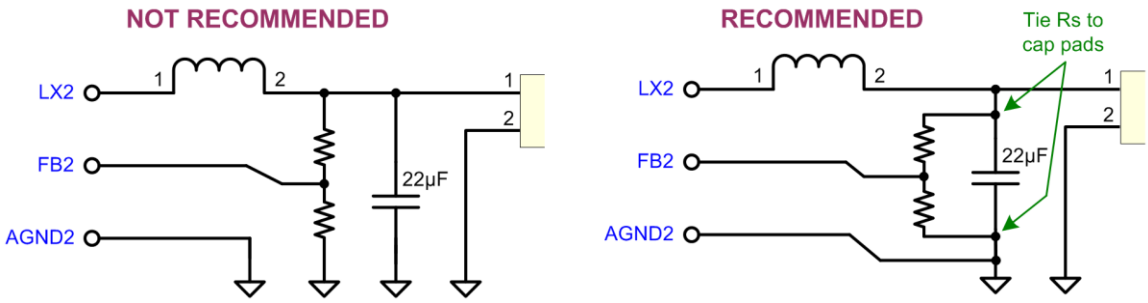


Figure 27 - Sense Line Design Practices

For Flyback Output 1, the same sense-line routing practices should be applied as described above for Outputs 2, 3 and 4. Since Output 1 requires an extra sense line (to measure secondary current), it is recommended that the three sense lines be run as shown in Figure 28, for optimum performance.

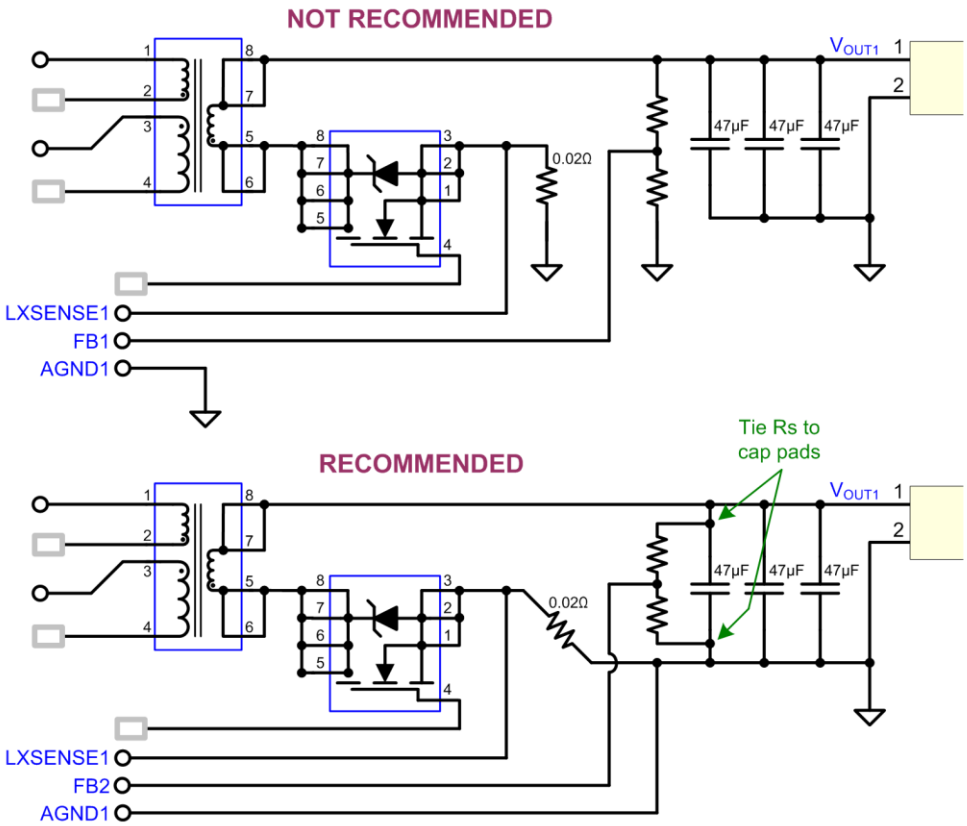


Figure 28 - Feedback Divider Design Practices

AS14X4 FOOTPRINT

The quad flat no-lead (QFN) package of the AS14x4 provides the advantages of near chip scale package size with very efficient thermal performance. By using the die attach pad of the package as the primary ground path and the direct path of thermal conduction and soldering the entire pad directly to the printed wire board (PWB), the electrical and thermal resistance of the package to the PWB is drastically reduced. Care must be taken to ensure the thermal path at the PWB interface can properly distribute the heat from the package into the bulk of the board.

Other considerations in the PWB design and assembly in regard to these packages involve PWB finish, pad design, solder mask coverage, via types, solder paste coverage of the signal pads and thermal pads, stencil design, solder joint quality, thermal profiling, and solder past type. Please refer also to "AN083: AX18x4 Assembly Guide" for more details on Kinetic' recommended best-practices for board-level PWB assembly of the AS14x4 product.

Electrically, the AS14x4 uses pads 1, 2 and 3 on the bottom of the device for electrical connectivity to their associated GND planes. Please make sure to short both the PGND pads on PWB. Thermally, these pads act as heat sinks. Therefore, by adding appropriate numbers of via's connecting each pad to multiple GND planes, excellent thermal and electrical performance can be achieved. Also, it is recommended to add a copper area with no solder mask on the bottom layer, for additional heat dissipation, as shown in Figure 29 below.

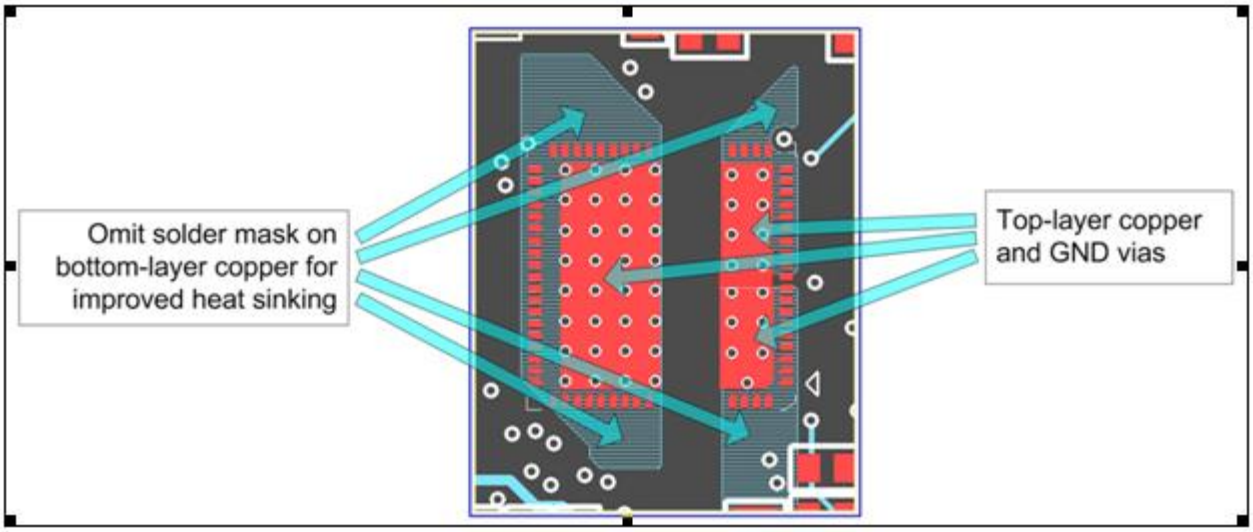


Figure 29 - AS14x4 Footprint Design Practices

SUMMARY

Proper electro-magnetic and thermal design practices enhance the performance and reliability of any Switching power supply design. Critical problems regarding layout, trace routing and noise coupling can be avoided with careful pre-layout planning. Designers are encouraged to contact Kinetic Technologies for guidance on design practices and testing procedures, to minimize or prevent (often hard-to-find) EMI problems in their printed-circuit board architecture.

Contact Information

Kinetic Technologies
6399 San Ignacio Ave, Suite 250,
San Jose, CA 95119
USA

Tel: (408) 746-9000 ext. 100
Website: www.kinet-ic.com

Important Notices

Legal Notice

Reference Design Policy

This document is provided as a design reference and Kinetic Technologies assumes no responsibility or liability for the information contained in this document. Kinetic reserves the right to make corrections, modifications, enhancements, improvements and other changes to this reference design documentation without notice.

Reference designs are created using Kinetic Technologies's published specifications as well as the published specifications of other device manufacturers. This information may not be current at the time the reference design is built. Kinetic Technologies and/or its licensors do not warrant the accuracy or completeness of the specifications or any information contained therein.

Kinetic does not warrant that the designs are production worthy. Customer should completely validate and test the design implementation to confirm the system functionality for the end use application. Kinetic Technologies provides its customers with limited product warranties, according to the standard Kinetic Technologies terms and conditions. For the most current product information visit us at www.kinet-ic.com

Life Support Policy

LIFE SUPPORT: KINETIC' PRODUCTS ARE NOT DESIGNED, INTENDED, OR AUTHORIZED FOR USE AS COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS. NO WARRANTY, EXPRESS OR IMPLIED, IS MADE FOR THIS USE. AUTHORIZATION FOR SUCH USE SHALL NOT BE GIVEN BY KINETIC, AND THE PRODUCTS SHALL NOT BE USED IN SUCH DEVICES OR SYSTEMS, EXCEPT UPON THE WRITTEN APPROVAL OF THE PRESIDENT OF KINETIC FOLLOWING A DETERMINATION BY KINETIC THAT SUCH USE IS FEASIBLE. SUCH APPROVAL MAY BE WITHHELD FOR ANY OR NO REASON.

“Life support devices or systems” are devices or systems which (1) are intended for surgical implant into the human body, (2) support or sustain human life, or (3) monitor critical bodily functions including, but not limited to, cardiac, respirator, and neurological functions, and whose failure to perform can be reasonably expected to result in a significant bodily injury to the user. A “critical component” is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Substance Compliance

With respect to any representation by Kinetic Technologies that its products are compliant with RoHS, Kinetic Technologies complies with the Restriction of the use of Hazardous Substances Standard (“RoHS”), which is more formally known as Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment. To the best of our knowledge the information is true and correct as of the date of the original publication of the information. Kinetic Technologies bears no responsibility to update such statements.